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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/648,150	08/16/00	EHBEN T	GR 98 P 5933

LERNER AND GREENBERG PA
POST OFFICE BOX 2480
HOLLYWOOD FL 33022-2480

MMC2/1024

EXAMINER	
NGUYEN, C	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)	
09/640,150	EHBEN et al.	
Examiner	Group Art Unit	
CUONG Q NGUYEN	2811	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-10 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 1-10 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 12/04/00 is acceptable.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. PCT/DE99/03829, filed on 12/01/1999.

Information Disclosure Statement

3. The Information Disclosure Statement filed on August 16, 2000 has been considered.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations "at least one second capacitive element is one of a plurality of second capacitive elements." in claim 3 (noted that in Fig.1 of present invention, there is only one second capacitive element formed by an interaction of second supply track (2) and a third supply track 3) and "at least one second capacitive element is formed by an interaction of said at least one third supply track and said first supply track" in claim 7 (noted that in Fig.1 of present invention, there is no capacitive element formed by an interaction of

at least one third supply track and first supply track) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dasgupta (US 6,146,939).

Regarding claims 1 and 5, Dasgupta discloses an integrated circuit comprising: a first supply track (340); a second supply track (325), wherein first and second supply tracks forming a first metallic layer; a second metallic layer formed above the first metallic layer having a third supply track (330) connected to the first supply track; a first capacitive element (C1) formed below the first metallic layer and is defined by a doped polysilicon layer (320) and a doping region (305, a n-well region) in a semiconductor substrate (300); the third supply track (330) and the second supply track (325) defined a second capacitive element (C3). See Dasgupta's Fig.3.

Dasgupta does not explicitly teach that the first supply track and third supply track connected to a first supply potential and the second supply track connected to a

second supply potential and at least one of first and second capacitive elements smoothing over the supply voltage.

It is known in the art that in order to operate an capacitor (to create a voltage potential), one plate of capacitor has to connect to a supply potential and another plate of capacitor has to connect to another supply potential.

Therefore, it would have been obvious to one of ordinary skill in the art to connect the first and third supply tracks to a first supply potential and the second supply track to a second supply potential as claimed in order to operate the capacitors (C1) and (C3).

It is noted that, the integrated circuit shown in Dasgupta's Fig.3 is identical as claimed integrated circuit. Therefore, it is inherent that at least one of first and second capacitive elements smoothing over the supply voltage as claimed.

Moreover, the limitation "at least one of first and second capacitive elements smoothing over the supply voltage." does not further define any structure limitation and is considered as a functional limitation. Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley,120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does ."(emphasis in original) Hewlett - Packard Co . v. Bausch & Lomb Inc ., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Regarding claim 2, as shown in Dasgupta's Fig.3, the first capacitive (C1) is connected in parallel with the second capacitive element (C3).

Regarding claim 3, as shown in Dasgupta's Fig.3, the first capacitive element (C1) is one of plurality of first capacitive elements (C1, C2) formed below both first supply track (340) and second supply track (325); the second capacitive element (C3) is one of plurality of second capacitive elements (C3, C4) wherein second capacitive element (C4) is formed between another second supply track (335) and the third supply track (330).

Regarding claim 4, as shown in Dasgupta's Fig.3 and TABLE 2, the first capacitive element (which is defined by the polysilicon layer (320) and the doping region (305)) in the semiconductor substrate (300) has a first capacitance much greater than a second capacitance of the second capacitive element (C3) (which is defined by the second supply track (325) and third supply track (330)) because a capacitor dielectric (350) of the first capacitive element is much thinner than a capacitor dielectric (365) of the second capacitive element. However, Dasgupta does not explicitly teaches that the first capacitance is greater than the second capacitance at least a factor of 10.

As taught by Dasgupta col.1 lines 10-25, capacitance of the capacitor structure is depended on the effective area, the permittivity of capacitor dielectric layer between the capacitor plates, and the thickness of capacitor dielectric layer. It is known in the art that these parameters are art recognized variable of importance which is subject to routine experimentation and optimization. Therefore, it would have been obvious to one of ordinary skill in the art to provide the effective area, the permittivity of capacitor

dielectric layer between the capacitor plates, and the thickness of capacitor dielectric layer so that the first capacitance is greater than the second capacitance at least a factor of 10.

Regarding claim 6, as shown in Dasgupta's Fig.3, an insulating material (360) formed between the polysilicon layer (320) and first, second supply tracks (340, 325), wherein the insulating material (360) having a plurality of plated-through holes formed therein connecting the first supply track to the polysilicon layer (320).

Regarding claim 7, as shown in Dasgupta's Fig.3, a layer (335) is considered as a third supply track, a layer (345) is considered as a second supply track and the layer (330) is considered as a first supply track, wherein a capacitive element (C4) is formed by an interaction of the third supply track (335) and the first supply track (330).

Regarding claim 8, as shown in Dasgupta's Fig.3, the capacitive element (C3) is formed by an interaction of the third supply track (330) and the second supply track (325).

Regarding claim 9, as shown in Dasgupta's Fig.3, the first capacitive elements (C1, C2) and second capacitive elements (C3, C4) have a capacitive component and a resistive component (noted that, every conductive layer has a resistive component). As above discussed, the first capacitive element (C1) connected in parallel to the second capacitive element (C3), where in the first capacitive element is formed by an interaction of the polysilicon layer (320) and the n-well region (305) in the

semiconductor substrate (300) and the second conductive element (C3) is formed by an interaction of the second supply track (325) and the third supply track (330). Therefore, it is inherent that in an equivalent circuit of a connection between the first and second capacitive elements the resistive component connected in series with the capacitive components, wherein the resistive component of second capacitive element substantially resulting from conductance of the first metallic layer (the second supply track 325) and the second metallic layer (the third supply tract 330); and the resistive component of first capacitive element substantially resulting from conductance of the polysilicon layer (320) and the doping region (n-well 305).

Regarding claim 10, as shown in Dasgupta's Fig.3, the resistive elements of n-well and polysilicon layer (320) are much greater than the resistive elements of metallic layers (325) and (330) because polysilicon material and doping region in the substrate have resistivities much higher than metal. However, Dasgupta does not explicitly teach that the resistive component of the first capacitive element is at least a factor of 10 greater than the resistive component of the second capacitive element.

It is known in the art that the first resistive component is depending on the dopants in the n-well and polysilicon layer. The dopants in the n-well and polysilicon layer are art recognized variable of importance which is subject to routine experimentation and optimization. Therefore, it would have been obvious to one of ordinary skill in the art to provide the resistive component of the first capacitive element

is at least a factor of 10 greater than the resistive component of the second capacitive element as claimed.

Conclusion

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

October 15, 2001